AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of processing pixel signals, the method comprising:

clamping a pixel readout line to a voltage level less than a voltage corresponding to a pixel signal;

subsequently coupling the pixel readout line to an output of a source-follower transistor and reading out the pixel signal onto the pixel readout line;

subsequently clamping a capacitive storage node in a pixel signal processing circuit to a voltage [[less]] higher than a voltage corresponding to the pixel signal appearing on the pixel readout line;

subsequently coupling the pixel readout line to the storage node in the processing circuit; and

storing a signal corresponding to the pixel signal that was read out on the capacitive storage node.

2. (Previously Presented) The method of claim 1, wherein clamping the pixel readout line comprises discharging a capacitance on the pixel readout line.

3. (Withdrawn) The method of claim 2, wherein discharging the pixel readout line is performed while processing a previously-stored pixel signal.

4. (Previously Presented) The method of claim 2, wherein the discharging the capacitance on the pixel readout line comprises disabling a pixel selection switch.

5. (Previously Presented) The method of claim 2, wherein the discharging the capacitance on the pixel readout line comprises enabling a switch to couple the pixel readout line to ground.

6. (Canceled)

7. (Previously Presented) The method of claim 1 wherein the storage node is clamped to substantially the same voltage and at about the same time as the pixel readout line.

8. (Previously Presented) The method of claim 1, further comprising:

resetting the pixel;

subsequently reading out a reset signal through the n-MOS source-follower; and

storing on a second capacitive storage node in the processing circuit a signal that corresponds to the reset signal.

9. (Previously Presented) The method of claim 8, further comprising:

prior to storing the signal corresponding to the reset signal, clamping the second capacitive storage node to a voltage less than the voltage corresponding to the reset signal; and

subsequently coupling the pixel readout line to the second storage node to store the signal corresponding to the reset signal on the second storage node.

10. (Withdrawn) The method of claim 1, further comprising passing the pixel signal that was read out through a p-MOS source-follower.

11. (Withdrawn) The method of claim 10, further comprising:

Clamping a capacitive storage node in a pixel signal processing circuit to a voltage greater than the pixel signal appearing at an input to the p-MOS source-follower, wherein the storage node is clamped before passing the pixel signal through the p-MOS source-follower to the processing circuit; and

subsequently coupling an output of the p-MOS source-follower to the storage node in the processing circuit.

12. (Withdrawn) The method of claim 11, further comprising:

resetting the pixel after storing the signal corresponding to the pixel signal in the processing circuit;

subsequently reading out a reset signal through the n-MOS source-follower;

passing the reset signal through the p-MOS source-follower to the processing circuit; and

storing a signal corresponding to the reset signal in the processing circuit.

13. (Withdrawn) The method of claim 12, wherein, prior to passing the reset signal through the p-MOS source-follower, a second capacitive storage node in the processing circuit is clamped to a voltage level higher than the reset signal appearing at the input to the p-MOS source-follower.

14. (Withdrawn) The method of claim 12, further comprising converting a difference between the pixel and reset signals stored by the processing circuit to a corresponding set of digital signals.

15. (Currently Amended) An imager comprising:

a pixel readout line;

an active pixel sensor comprising a source-follower transistor through which signals sensed by the sensor can be read out to the pixel readout line, a first switch that can be enabled to read out signals from the sensor, and a reset switch;

a signal processing circuit that can be coupled to the pixel readout line; and

a controller configured to provide control signals to cause the pixel readout line to be clamped to a voltage level less than a voltage corresponding to a signal sensed by the sensor, and subsequently to cause the sensor signal to be read out through the source-follower transistor to the pixel readout line and to be stored by the processing circuit,

wherein the processing circuit comprises a capacitive storage node, and

wherein the controller is <u>further</u> configured to provide control signals to <u>subsequently</u> cause the capacitive storage node to be clamped to a voltage [[less]] <u>higher</u> than a voltage corresponding to the sensor signal appearing on the pixel readout line, and subsequently to cause the pixel readout line to be coupled to the storage node.

16. (Withdrawn)

17. (Previously Presented) The imager of claim 15, further comprising:

a third switch coupled between the pixel readout line and ground,

wherein the controller is configured provide a control signal to cause the pixel readout line to be clamped by enabling the third switch.

18. (Canceled)

19. (Previously Presented) The imager of claim 15, wherein the storage node is clamped to substantially the same voltage and at about the same time as the pixel readout line.

20. (Previously Presented) The imager of claim 15, wherein:

the processing circuit further comprises a second capacitive storage node, and

the controller is configured to provide control signals to cause the reset switch in the pixel to be enabled, and subsequently to cause a reset signal to be read out onto the pixel readout line through the source-follower transistor, and to cause a signal that corresponds to the reset signal to be stored on the second capacitive storage node.

21-39. (Canceled)

40. (Previously Presented) The method of claim 1, wherein the reading out the pixel signal onto the pixel readout line comprises reading out the pixel signal through the source-follower transistor.

41. (Previously Presented) The method of claim 40, wherein the source-follower transistor comprises an n-MOS transistor.

42. (New) The method of claim 1, wherein the capacitive storage node comprises a binary scaled capacitor network.

43. (New) The imager of claim 15, wherein the capacitive storage node comprises a binary scaled capacitor network.